

# Design Rules Alumina 96% PCB (Al<sub>2</sub>O<sub>3</sub> 96%)



- 1. Definitions
  - 1.1. Production solutions:
  - 1.2. Metalizations
  - 1.3. Classifications
- 2. C-Proto
  - 2.1. DPC
    - 2.1.1. Dimensional specifications
    - 2.1.2. Metalization & finish
    - 2.1.3. Spacing & vias
    - 2.1.4. Tolerances
  - 2.2. Thick film
    - 2.2.1. Dimensional specifications
    - 2.2.2. Metalization & finish
    - 2.2.3. Spacing & vias
    - 2.2.4. Tolerances
- 3. C-Production
  - 3.1. DPC
    - 3.1.1. Dimensional specifications
    - 3.1.2. Metalization & finish
    - 3.1.3. Spacing & vias
    - 3.1.4. Tolerances
  - 3.2. Thick film
    - 3.2.1. Dimensional specifications
    - 3.2.2. Metalization & finish
    - 3.2.3. Spacing & vias
    - 3.2.4. Tolerances

## 1. Definitions

### 1.1. Production solutions:

CERCuits offers two production solutions for Aluminum Oxide 96% (Al<sub>2</sub>O<sub>3</sub> 96%) circuits:

**C-proto** is our solution tailored for low-volume manufacturing batches, primarily produced in Belgium using our unique process. We recommend this solution for order sizes ranging from 1 to 10 panels per design.

A single C-proto manufacturing panel has a standard usable surface of 100x80mm.

**C-production** is designed for medium to high-volume manufacturing batches and will mostly be produced through one of our high-volume production partners. We recommend this solution for orders exceeding 10 manufacturing panels per design.

A single C-production manufacturing panel has a standard usable surface of 115x115mm.

## 1.2. Metalizations

Both manufacturing solutions can be supplied using two different methods of metallization:

**Direct Plated Copper (DPC)** utilizes copper as a conductor. After sputtering an interface and seed layer, copper is plated to the desired thickness. This manufacturing method closely resembles traditional printed circuit board production and supports plated-through holes, as well as similar solder masks and surface finishes such as ENIG & ENEPIG.

**Thick Film technology** typically employs silver or silver-palladium as a conductor, which is screen printed onto the substrate using a paste. The printed conductor is then dried and fired at high temperatures to form a robust bond. While this technology is well-suited for high-temperature applications exceeding 300°C, it does have limitations, including restricted possibilities for plated-through holes and surface finishes.

Both technologies can be assembled using soldering or wire bonding with the appropriate surface finish. For further details on surface finish selection, please feel free to contact us.

## 1.3. Classifications

Our design rules are classified into two categories:

**Standard:** Adhering to these specifications generally results in a smooth production process with reduced chances of failures or remakes. This approach leads to quicker turnaround times and lower costs.

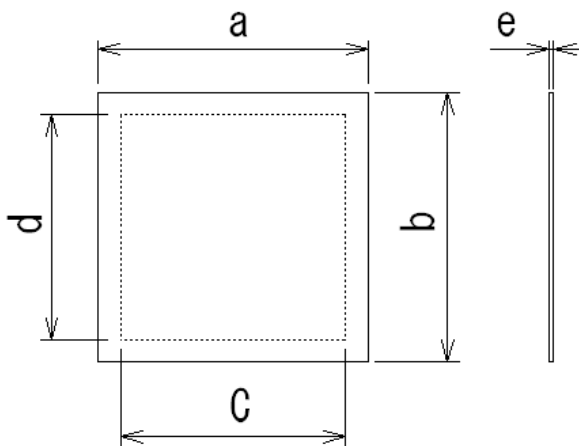
**Special:** These specifications push the boundaries of the production process and could potentially lead to challenges. While we can still likely fulfill these orders, additional engineering and/or production adjustments might be required for successful fabrication. Consequently, lead times and costs are higher in such cases. We also might ask for design/specification updates before or during manufacturing.

## 2. C-Proto

### 2.1. DPC

Note: C-Proto has no Tooling & Non recurring engineering costs

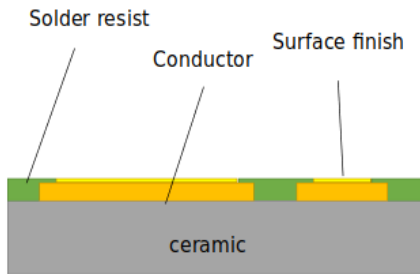
#### 2.1.1. Dimensional specifications



Parameter	Standard	Special	Unit
Panel dimensions a & c	100	\	mm

<b>Panel dimensions b &amp; d</b>	80	\	mm
<b>Panel dimension e</b>	0.38   0.5   0.635   0.76   1.0	0.25   1.5	mm
<b>Min. dimension</b>	5 x 5	1 x 1	mm

### 2.1.2. Metalization & finish

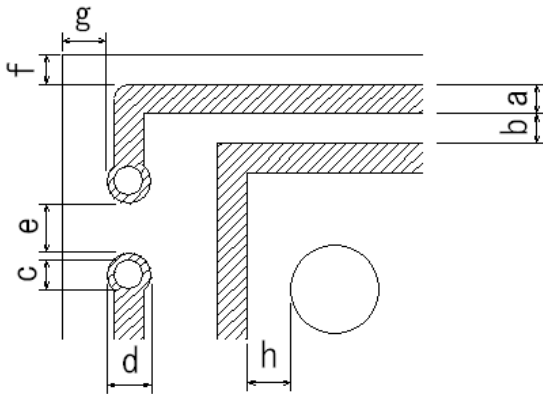


Parameter	Standard	Special	Unit
<b>Conductor</b>	Copper - Cu	\	
<b>Conductor thickness</b>	18   35   70	other thicknesses between 10um-105um	µm
<b>Surface finish</b>	None, Immersion Tin (Sn), ENIG, ENEPIG  (see lookup table below)	Immersion Ag, EPIG, DIG, Hard gold  (see lookup table below)	
<b>Solder resist</b>	Green, White, Black, High reflective white	UV-C reflective mask (>80% reflectance at 200-280nm)	
<b>Solder resist minimum opening</b>	0.15	0.08	mm
<b>Solder resist minimum pad overlap</b>	0.05	\	mm
<b>Silk screen / legend</b>	Engraving only	\	
<b>Layers</b>	single or double-sided	\	

Surface Finish lookup table

Copper thickness / line spacing	50um	75um	100 um	150um	200um-
18um	DIG, immersion Tin, immersion Ag	EPIG, DIG, Immersion Ag, Immersion Tin	EPIG, DIG, Immersion Ag, Immersion Tin, Hard gold	ENEPIG, ENIG, EPIG, DIG, Immersion Ag, Immersion Tin, Hard Gold	ENEPIG, ENIG, EPIG, DIG, Immersion Ag, Immersion Tin, Hard gold
35um	/	DIG, immersion Tin, immersion Ag			
70um and above	/	/	DIG, immersion Tin, Immersion Ag	DIG, Immersion Ag, Immersion Tin	

### 2.1.3. Spacing & vias



Parameter	Standard	Special	Unit
Min. line width (a)	0.15	0.05	mm
Min. line spacing (b)	0.15	0.05	mm
Line/pad to edge spacing (f)	0.2	0.05	mm
Line to hole/via spacing (h)	0.15	0.05	mm
Edge metalization	no	Yes	
<b>Via specifications</b>			
Min. via diameter (c)	0.3mm (thickness=<1mm)	0.15(thickness <0.38mm) - 0.2 (thickness <0.5mm)	mm

<b>Min. via spacing</b>	0.5	0.3	mm
<b>Via/hole to edge spacing</b>	3x Via diameter	1x Via diameter	mm
<b>Through hole metallisation</b>	Plated vias, plugged vias	copper filled vias (dia 0.15-0.3mm)	\
<b>Filled via Size</b>	\	0.15-0.3	mm
<b>Annular ring specifications</b>			
<b>Min. annular ring diameter (d)</b>	via diameter +0.4	via diameter +0.2	mm
<b>Min. annular ring spacing (e)</b>	0.2	0.1	mm
<b>Annular ring to edge spacing (g)</b>	0.2	0.05	mm

#### 2.1.4. Tolerances

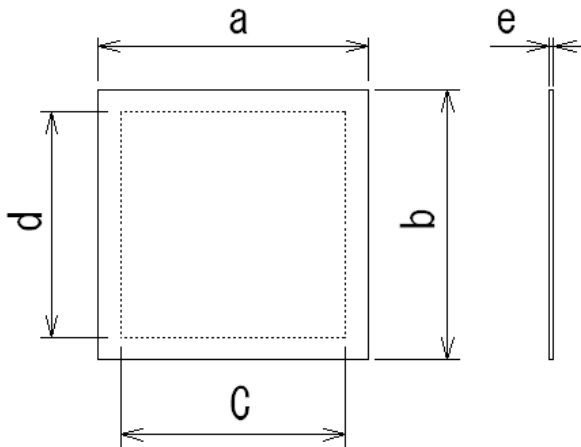
<b>Parameter</b>	<b>Standard</b>	<b>Special</b>	<b>Unit</b>
<b>Dimensional tolerance</b>	+/- 100	+/- 50	µm
<b>Thickness tolerance</b>	+/- 10	+/- 5	%
<b>Hole tolerance</b>	+/- 100	+/- 50	µm
<b>Pad to hole/via tolerance</b>	+/- 100	+/- 50	µm
<b>Conductor thickness tolerance</b>	+/- 6	\	µm
<b>Line/Space width tolerance</b>	+/- 50	+/- 30	µm

<b>Surface roughness ceramic (Ra)</b>	\	Ra <0.3	μm
<b>Misalignment (only for double sided)</b>	≤200	≤100	μm

## 2.2. Thick film

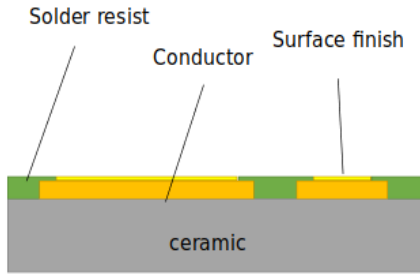
Note: C-Proto has no Tooling & Non recurring engineering costs

### 2.2.1. Dimensional specifications



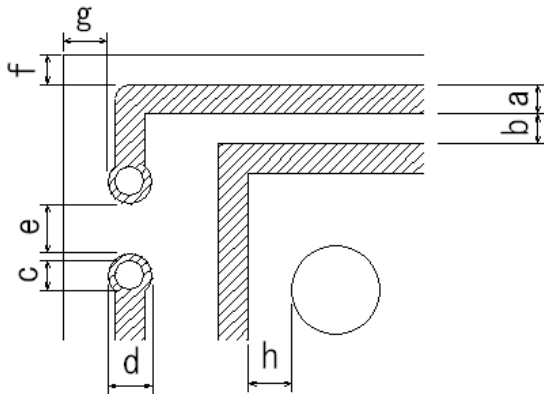
Parameter	Standard	Special	Unit
<b>Panel dimensions a &amp; c</b>	100	\	mm
<b>Panel dimensions b &amp; d</b>	80	\	mm
<b>Panel dimension e</b>	0.38   0.5   0.635   0.76   1.0	0.25   1.5   2.0	mm
<b>Min. dimension</b>	5 x 5	1 x 1	mm

### 2.2.2. Metalization & finish



Parameter	Standard	Special	Unit
<b>Conductor</b>	Silver - Ag, Silver-Palladium - AgPd (5% Pd)	Silver-Palladium - AgPd (10% Pd or other %)	
<b>Conductor thickness</b>	10-15	20-24, please enquire for other thicknesses	μm
<b>Surface finish</b>	none (Ag or AgPd)	Galvanic NiAu, Galvanic Au	
<b>Solder resist</b>	Blue dielectric (glass-based)	Green dielectric (glass-based)	
<b>Solder resist minimum opening</b>	0.2	0.1	mm
<b>Solder resist minimum pad overlap</b>	0.1	0.05	mm
<b>Silk screen / legend</b>	Engraving only	\	
<b>Layers</b>	single or double-sided	3   4 layers	

### 2.2.3. Spacing & vias



Parameter	Standard	Special	Unit
Min. line width (a)	0.2	0.1	mm
Min. line spacing (b)	0.15	0.1	mm
Line/pad to edge spacing (f)	0.15	0.1	mm
Line to hole/via spacing (h)	0.15	0.1	mm
Edge metalization / Castellated holes	no	yes	
<b>Via specifications</b>			
Via diameter (c)	0.2-0.4	>1mm plated vias only	mm
Min. via spacing	0.5	0.5	mm
Via/hole to edge spacing	3x Via diameter	1x Via diameter	mm
Through hole metallisation	Filled vias	Plated via	\
Filled via Size	0.2-0.4	\	mm
<b>Annular ring specifications</b>			
Min. annular ring diameter (d)	via diameter +0.4	via diameter +0.2	mm
Min. annular ring spacing (e)	0.2	0.1	mm
Annular ring to edge spacing (g)	0.2	0.1	mm



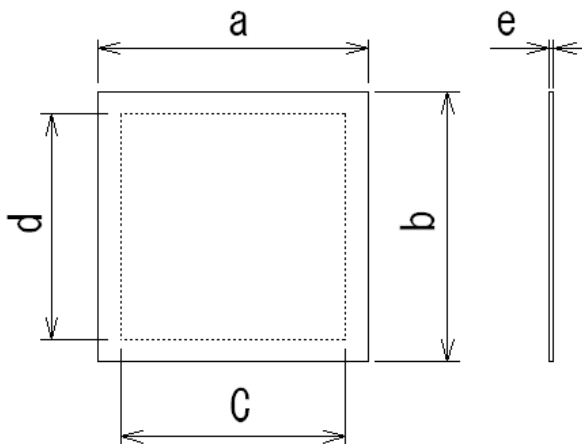
### 2.2.4. Tolerances

Parameter	Standard	Special	Unit
Dimensional tolerance	+/- 100	+/- 50	μm
Thickness tolerance	+/- 10	+/- 5	%
Hole tolerance	+/- 100	+/- 50	μm
Pad to hole/via tolerance	+/- 100	+/- 50	μm
Conductor thickness tolerance	+/-6	\	μm
Line/Space width tolerance	+/- 50	+/- 40	μm
Surface roughness ceramic (Ra)	\	Ra <0.4	μm
Misalignment (only for double-sided)	≤200	≤100	μm

## 3. C-Production

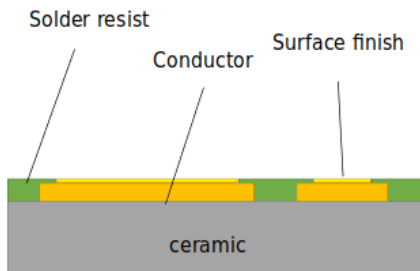
### 3.1. DPC

#### 3.1.1. Dimensional specifications



Parameter	Standard	Special	Unit
<b>Panel dimensions a &amp; c</b>	120	\	mm
<b>Panel dimensions b &amp; d</b>	120	\	mm
<b>Panel dimension e</b>	0.25   0.38   0.5   0.635   0.76   1.0   1.5	2.0   3.0	mm
<b>Minimum dimension</b>	2x2	1x1	mm

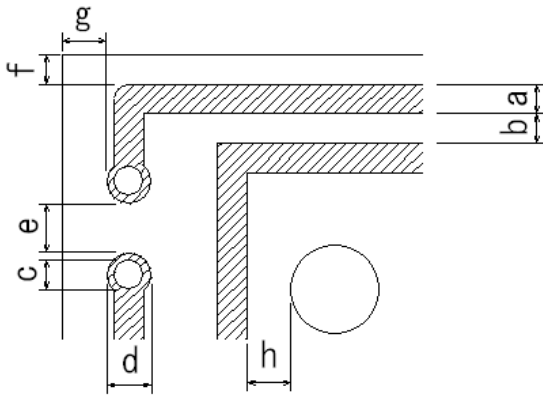
### 3.1.2. Metalization & finish



Parameter	Standard	Special	Unit
<b>Conductor</b>	Copper - Cu	\	
<b>Conductor thickness</b>	18   35   70	Other thickness between 10 - 300	μm
<b>Surface finish</b>	Imm. Ag, ENIG, ENEPIG	EPIG, Hard Gold, OSP	
<b>Solder resist</b>	Green, White, Blue, Black	other colors	
<b>Solder resist minimum opening</b>	0.2	0.08	mm
<b>Solder resist minimum pad overlap</b>	0.1	0.05	mm
<b>Silk screen / legend</b>	black, white	other colors	

<b>Silk screen / legend size</b>	W: 0.1 - H: 0.7	\	mm
<b>Layers</b>	single or double sided	\	

### 3.1.3. Spacing & vias



Parameter	Standard	Special	Unit
<b>Min. line width (a)</b>	0.15	0.08	mm
<b>Min. line spacing (b)</b>	0.15	0.08	mm
<b>Line/pad to edge spacing (f)</b>	0.2	0.1	mm
<b>Line to hole/via spacing (h)</b>	0.2	0.1	mm
<b>Edge metalization / castellated holes</b>	yes		
<b>Via specifications</b>			
<b>Min. via diameter (c)</b>	0.1 (aspect ratio 1:7)	0.06	mm
<b>Min. via spacing</b>	0.3	0.2	mm
<b>Via/hole to edge spacing</b>	3x Via diameter (c)	castellated holes possible	mm

<b>Through hole metallisation</b>	PTH, plugged vias	copper filled vias (dia 0.08-0.2mm)	\
<b>Filled via Size</b>	\	0.1-0.3	mm
<b>Annular ring specifications</b>			
<b>Min. annular ring diameter (d)</b>	0.2	0.1	mm
<b>Min. annular ring spacing (e)</b>	0.15	0.08	mm
<b>Annular ring to edge spacing (g)</b>	0.15	\	mm

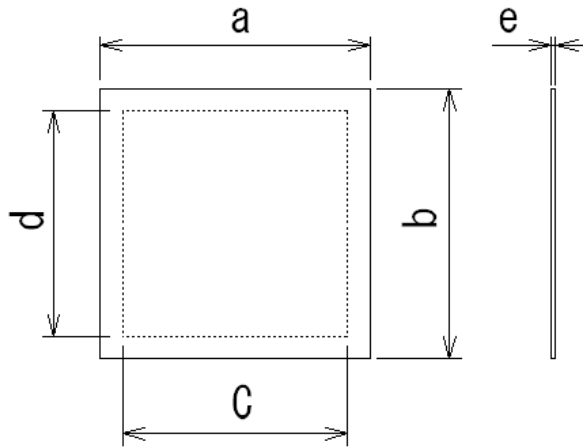
#### 3.1.4. Tolerances

<b>Parameter</b>	<b>Standard</b>	<b>Special</b>	<b>Unit</b>
<b>Dimensional tolerance</b>	+/- 100	+/- 50	µm
<b>Thickness tolerance</b>	+/- 10	+/- 5	%
<b>Hole tolerance</b>	+/- 100	+/- 50	µm
<b>Pad to hole/via tolerance</b>	+/- 100	+/- 50	µm
<b>Conductor thickness tolerance</b>	+/- 6 (thickness 35µm)	please enquire	µm
<b>Line/Space width tolerance</b>	+/- 20	\	µm
<b>Surface roughness ceramic (Ra)</b>	Ra ≤ 0.3 Rz ≤ 2	please enquire	µm
<b>Misalignment (only for double sided)</b>	≤ 100	≤ 50	µm

### 3.2. Thick film

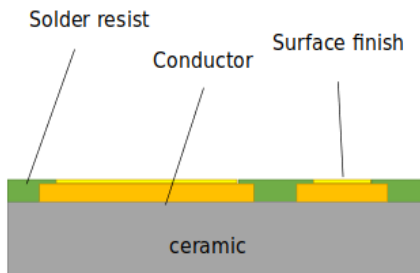
Note: NRE & tooling costs are required for screen manufacturing and process optimization

#### 3.2.1. Dimensional specifications



Parameter	Standard	Special	Unit
Panel dimensions a & c	115	125	mm
Panel dimensions b & d	115	125	mm
Panel dimension e	0.38   0.5   0.635   0.76   1.0	0.25	mm
Min. dimension	5 x 5	1 x 1	mm

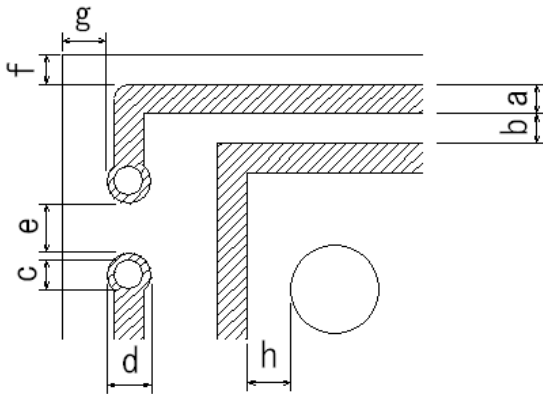
#### 3.2.2. Metalization & finish



Parameter	Standard	Special	Unit
Conductor	Silver - Ag, Silver-Palladium - AgPd	Silver-Platinum	
Conductor thickness	10-20	20-40	µm

<b>Surface finish</b>	none	\	
<b>Solder resist</b>	White, Blue & Black (glass-based)	High reflective white	
<b>Solder resist minimum opening</b>	0.2	0.1	mm
<b>Solder resist minimum pad overlap</b>	0.1	0.1	mm
<b>Silk screen / legend</b>	Black, White	\	
<b>Layers</b>	single or double-sided	3   4 layers	

### 3.2.3. Spacing & vias



Parameter	Standard	Special	Unit
<b>Min. line width (a)</b>	0.2	0.1	mm
<b>Min. line spacing (b)</b>	0.2	0.1	mm
<b>Line/pad to edge spacing (f)</b>	0.15	0.1	mm
<b>Line to hole/via spacing (h)</b>	0.15	0.1	mm
<b>Edge metalization / Castellated holes</b>	no	yes	

<b>Via specifications</b>			
<b>Via diameter (c)</b>	0.12-0.3	>1mm plated vias only	mm
<b>Min. via spacing</b>	0.5	0.5	mm
<b>Via/hole to edge spacing</b>	3x Via diameter	1x Via diameter	mm
<b>Through hole metallisation</b>	Filled vias	Plated via	\
<b>Filled via Size</b>	0.12-0.3	\	mm
<b>Annular ring specifications</b>			
<b>Min. annular ring diameter (d)</b>	via diameter +0.4	via diameter +0.2	mm
<b>Min. annular ring spacing (e)</b>	0.2	0.15	mm
<b>Annular ring to edge spacing (g)</b>	0.2	0.15	mm

#### 3.2.4. Tolerances

<b>Parameter</b>	<b>Standard</b>	<b>Special</b>	<b>Unit</b>
<b>Dimensional tolerance</b>	+/- 100	+/- 50	µm
<b>Thickness tolerance</b>	+/- 10	+/- 5	%
<b>Hole tolerance</b>	+/- 100	+/- 50	µm
<b>Pad to hole/via tolerance</b>	+/- 100	+/- 50	µm
<b>Conductor thickness tolerance</b>	+/-4 (10um thickness), +/-8 (20um thickness)	\	µm

<b>Line/Space width tolerance</b>	+/- 50	+/- 40	μm
<b>Surface roughness ceramic (Ra)</b>	\	Ra <0.5	μm
<b>Misalignment (only for double-sided)</b>	≤100	≤50	μm